Outline

I. Hard Disk Drives
   1. Data Storage Industry --- still alive and thriving
   2. Short History of Magnetic Recording
   3. A look inside the HDD
   4. Head and Media Technology
   5. Energy-Assisted Recording Technology for the Future
      • Heat-Assisted Magnetic Recording (HAMR)
      • Microwave-Assisted Magnetic Recording (MAMR)

II. Magnetic Random Access Memory
   1. Comparison of Memory Technologies
   2. Basics of Spin-Transfer Torque MRAM and Challenges
   3. Other MRAM approaches: SOT-MRAM, VCMA
Need to continue increasing storage density of HDDs (cost/space/power)
Diverse and Connected Data Types

*Tight coupling between Big Data and Fast Data*

Big Data
- INSIGHT
- PREDICTION
- PRESCRIPTION

Scale

Fast Data
- MOBILITY
- REAL-TIME RESULTS
- SMART MACHINES

Performance

Batch Analytics

Data Aggregation

Streaming Analytics

Machine Learning

Artificial Intelligence

Modeling

*ALGORITHMS*

*DATA*
Insatiable Growth in Data

HDDs continue to play an important role in the future of data storage

By 2020

~70% of the ~10 ZBs stored will still reside on HDDs

~90% in data centers

1 ZB = 10^{21} bytes
or
1 billion 1TB drives

1 ZB = 10^{21} bytes

Source: WDC Analysis
Market Glance:

- 94M HDD shipped in 1st quarter 2018
- Total exabytes shipped is increasing.
- Number of drives decreasing.
- Average HDD cost ~$60

Source: Coughlin Assoc
Hard Disk Drive
History of HDDs

1956

RAMAC - first HDD
- 5 MegaBytes
- Fifty 24” disks
- 2 kbits/in²
- $10,000/Mbyte

1980’s – 1990’s

Towards smaller form factors

Model 3340 hard disk

Apple iPOD
- 160 GigaBytes
- Two 1.8” disks
- 3600 RPM
- 228 Gbits/in²
- 52 MBytes/s

The trend to ever smaller HDD’s has stopped though.
HDD vs. Flash SSD $/TB Annual Takedown Trend

MAMR will enable continued $/TB advantage over Flash SSDs

Source: WDC Analysis
1 disk, 1 or 2 heads
Typical Components in a Modern Disk Drive

- **Spindle Motor & Disk Clamp**: holds and spins disks
- **Load/Unload Ramp**: parks head off media during non-use
- **Actuator Voice Coil Magnets**: positions the heads
- **Actuator**: positions the heads
- **Suspension**: holds suspended heads, provides electrical connections from head to flex cable
- **Filter**: cleans air
- **Disk Enclosure**: provides electrical connection from suspension to electronic card
- **Disk(s)**: stores written information
- **Head(s)**: writes and reads data
- **Electronic Card**: provides data interface to disk controller
  - Control operation of disk drive (spindle, actuator, position servo)
  - Encodes written data and decodes read back data
  - Provide read/write signals to heads via flex cable

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What’s in the drive?

Magnetic recording system

- Reader
- Writer
- CPP sensor
- Media
- Air bearing
- Trackwidth
- Data tracks
- Track density (kilotrack / inch = ktpi)
- Bit density (kilobit / inch = kbpi)
- Areal Density = \( kbpi \times ktpi = \text{Giga-bit/in}^2 \)
- Typical is 2 disks & 4 heads for laptop-HDD
Most straightforward method to increase storage bit density is to **shrink everything**
→ **scale down** (head dimensions, media thickness, media grain size, head-media spacing, etc…)
Must maintain **signal-to-noise ratio** while scaling
→ **New technologies to boost signal and/or reduce noise**
  (Ex: Longitudinal recording → perpendicular; Anisotropic magnetoresistive sensor → giant magnetoresistive sensor)
The HDD Head: Extreme Close-up

Sliders on a Dime

“Slider”
Read/Write Elements
~1000 process steps
Air Bearing Surface

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Head-Disk Interface

- **Read Head**
  - NiFe shield
  - Read gap ~20 nm
  - Read element free-layer ~4 nm
  - MgO tunnel junction (TMR ratio 50-100%)
  - Pinned reference-layer

- **Disk**
  - Recording Medium (Magnetic Layer) ~15 nm
  - Lube ~1 nm
  - Roughness ~0.5 nm
  - Carbon Overcoat ~2 to 3 nm
  - Air or Helium

- Clearance < 1 nm
- Disk velocity 
  - ~30 m/s → 70 mi/hr

R. Wood, ISPS 2016
Today ~700Gb/in² (now 1Tb/in²), HMS ~8-10nm, BL ~15nm, SCALED × 10⁶

- **Disk** = SF Bay Area (95 km dia)
  - 1 bit = 1 finger (1.5 × 8cm)
- **Head** = Boeing 787
- **Fly speed @ O.D.**
  - = 7200 rpm × 300 km
  - = 0.12 c
    - (c = 3 × 10⁸ m/s)
- **Fly height = 5mm**

- HDD × 1 million = “a Boeing 787 flying at 12% of the speed of light (at disk’s O.D.) 5mm above a 95 km wide disk and seeking, reading and writing bits of information the size of a human’s finger”
Helium-Sealed HDDs

- 2013: First helium-sealed drive from HGST, 6TB Ultrastar He6 had 5 disks
- Breakthrough in sealing the helium in the drive
- Current generation: 14TB, Ultrastar He14 has 8 disks
- Advantage of He: less drag → less power & less noise. Thinner disks, pack in more disks → higher capacity drives

Source: blog.westerndigital.com
What is it? And why is it here?
Western Digital's HGST 8TB helium-filled drives were used, whereas capacity and cost limitations ruled out SSDs.

They wrote time-slice data using a round-robin algorithm across the 32 hard drives. These drives are mounted in groups of eight in four removable modules.

The low ambient air density at the telescope sites necessitated sealed, helium-filled hard drives, both for the system disk for recorders and also in all the data recording modules. Ordinary air-filled drives crashed when tried out in 2015; the air was too thin to provide the cushion needed to support the heads.
Microactuator

Figure 1. WDMA structure and actuation

Data tracks
Trackwidth

"UP" bit

"DOWN" bit

Bit density
(kilobit / inch = kbpi)

~ 50 nm

Piezo

Flexure

Stroke

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Read/write heads:
1 wafer (150 or 200 mm)
has ~100,000 heads
Wafer spends 4 months in the fab

Media:
20-24 sputter chambers
Sputter output ~ 800-1500 disks/hour
→ new disk every 3.5 sec
## Read Head Sensor Technologies

<table>
<thead>
<tr>
<th>Year</th>
<th>1&lt;sup&gt;st&lt;/sup&gt; Density (Gb/in&lt;sup&gt;2&lt;/sup&gt;)</th>
<th>Sensor Technology</th>
<th>Structure</th>
<th>MR Effect</th>
<th>Sense Current Geometry</th>
</tr>
</thead>
<tbody>
<tr>
<td>1979</td>
<td>0.01 Gb/in&lt;sup&gt;2&lt;/sup&gt;</td>
<td>Thin-film Inductive</td>
<td><img src="image" alt="Thin-film Inductive Structure" /></td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>1991</td>
<td>0.1 Gb/in&lt;sup&gt;2&lt;/sup&gt;</td>
<td>MR Sensor</td>
<td><img src="image" alt="MR Sensor Structure" /></td>
<td>Anisotropic</td>
<td>CIP</td>
</tr>
<tr>
<td>1997</td>
<td>2 Gb/in&lt;sup&gt;2&lt;/sup&gt;</td>
<td>Spin Valve</td>
<td><img src="image" alt="Spin Valve Structure" /></td>
<td>Giant MR</td>
<td>CIP</td>
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<tr>
<td>2006</td>
<td>100 Gb/in&lt;sup&gt;2&lt;/sup&gt;</td>
<td>Tunnel Valve</td>
<td><img src="image" alt="Tunnel Valve Structure" /></td>
<td>Tunneling</td>
<td>CPP</td>
</tr>
<tr>
<td>?</td>
<td>&gt;1Tb/in&lt;sup&gt;2&lt;/sup&gt;</td>
<td>?</td>
<td>?</td>
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<td>?</td>
</tr>
</tbody>
</table>
The edges of each recorded bit follow the grain boundaries → edge noise

For smaller bits (higher density), need smaller grain sizes to avoid increasing noise

→ Scale media microstructure together with rest of recording system

500 Gb/in²: bit size ~ 15 nm x 65 nm

SNR \propto \frac{B}{D} \sqrt{\frac{R_w}{D}}

B=bit length
D=grain diameter
R_w=reader width

\langle D \rangle = 8.5 \text{ nm } +/- 2.5 \text{ nm}
Data Density, Grain Size, and Thermal Stability

stored magnetic energy $\propto$ anisotropy x volume
thermal energy $\propto$ temperature and time

\[ \frac{K_u V}{k_B T} \]

• to increase density, need to scale grains smaller
• smaller grains are thermally unstable (data erases itself!)

SOLUTIONS:
• improved writability (perpendicular media)
• work with larger grains: patterned media
• work with higher anisotropy: energy assisted recording
Perpendicular Magnetic Recording (PMR)

- Essential to continued areal density growth
  - Higher head fields, higher coercivity, thicker media, greater thermal stability
  - First product introductions in 2005 and 2006

- All HDD are perpendicular.
- Media is part of write head.
- Enabled new media technology, such as exchange spring
Grain size has been constant since PMR was introduced, but density still increased 5-fold from 150-750 Gb/in².

Progress via reduction in magnetic cluster size and distribution (lateral exchange) by using a multi-layered media structure.

Grain boundary, w~1nm

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Why Grain Size has not decreased

When using smaller grain Ru to reduce CoCrPt grain pitch,
- thinner grains boundaries
- more lateral exchange between grains
- larger magnetic cluster size (measured by MFM, scattering, loops,...)
- negates benefit of smaller grains, and also leads to larger exchange distribution

![Graph showing magnetic cluster size vs grain pitch](image)

- Thin boundary
- medium boundary
- Thick boundary

![Normalized Cluster Size graph](image)

- GP ≈ 7 nm
- GP ≈ 8 nm
- GP ≈ 9 nm

Normalized Cluster Size = Cluster Size / GP
Exchange Control Layers

Solution to actually reducing grain size from here on:

➔ reduce grain core, fixed boundary thickness
➔ maintains cluster size, but reduces thermal stability
  ➔ need to increase Ku
  ➔ too hard to write
  ➔ reduce vertical exchange to allow more incoherent rotation, also reduced lateral exchange in cap
➔ But, reduced lateral exchange also increases distributions!
SAXS Study of PMR Media (distributions)

MCL = Magnetic Cap Layer, GRL = Granular Recording Layer

Gen 1
~ 150 Gb/in² (2006)

Gen 2

Gen 3

Gen 4
~ 700 Gb/in² (2012)

MCL + GRL / GRL only
- Struct. grain
- Mag. cluster

Add MCL

ECL-1
G3 Oxide
G2 Oxide
G1 High Ku Oxide
Onset Layers
Ru
Voronoi growth will have ~22% size distribution
- Random grain seeds, isotropic 2D growth
- Exchange exponential in boundary thickness

How can we better define grain nucleation sites?
Templated growth of BPM

1. Shallow topographic template
   - patterned layer
   - substrate
   - ~3 nm

2. Underlayer nucleation and growth

3. Co-sputtering of mag alloy and segregant

- Other in following years
Templated Bit Patterned Media

After several cycles of learning

Innovation: Pattern crystalline Pt pillar. Grow Ru on top of it

En Yang et al., *Nano Lett.* 15, 4726 *(2016)*
Search for Naturally Ordered Nucleation Sites

LogNormal
$R^2 = 99.0\%$
$\Sigma D/D = 13.4\%$
TEM Evidence of Templating Effect

$\sigma_{D/D} = 8.03\%$

EFTEM, red=Fe

nanoparticles
Storage Trilemma: SNR, thermal stability, writability

\[
\frac{\text{energy barrier}}{\text{thermal energy}} \propto \frac{\text{anisotropy x volume}}{k_B \times \text{temperature}} = \frac{K_u V}{k_B T}
\]

\[
SNR \propto \frac{B}{D} \sqrt{\frac{R_W}{D}}
\]

B=bit length
D=grain diameter
R_w= reader width

\[H_{\text{head}} \sim H_k, \text{media} \sim K_u\]

The problem:
To increase SNR, need small grains.
Small grains are thermally unstable.
To avoid thermal instability, increase grain anisotropy Ku.
Increasing Ku increasing media Hc and makes the medium more difficult to write.
Overcoming the Trilemma

Shingled Magnetic Recording (SMR)

Heat Assisted Magnetic Recording (HAMR)

Microwave Assisted Magnetic Recording (MAMR)

Two Dimensional Magnetic Recording (TDMR)

More on these today
Energy Assisted Magnetic Recording: MAMR and HAMR

- Microwave fields emitted by a Spin Torque Oscillator (STO) allows writing higher coercivity media
- Heat from laser allows writing higher coercivity media

<table>
<thead>
<tr>
<th>MAMR</th>
<th>HAMR</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD</td>
<td>Zhu(^1): 4 Tb/in(^2)</td>
</tr>
<tr>
<td>Media</td>
<td>Grain=4.5nm, Hk=40kOe, KuV/kT=60</td>
</tr>
<tr>
<td>Head</td>
<td>STO=45nmx12nm, 35GHz ideal in-plane rot.</td>
</tr>
</tbody>
</table>

DOI: [10.1109/TMAG.2013.2285215](https://doi.org/10.1109/TMAG.2013.2285215)

[https://doi.org/10.1063/1.4953231](https://doi.org/10.1063/1.4953231)
Spin Torque Oscillator (STO)

- Leveraging the progress of spintronic technology, STO is the most critical development area in MAMR application.
MAMR Working Principles

- STO generates an AC magnetic field.
- AC field assists media switching via media FMR (Ferromagnetic resonance)
- Media structure tuned for optimum frequency response
- MAMR technology enables writing of high Hk media.
Microwave Assisted Recording (MAMR)

J. Zhu, Carnegie Mellon Univ.

STO: LLG + spin transfer

\[
\frac{\partial \mathbf{m}}{\partial t} = -\gamma (\mathbf{m} \times \mathbf{H}_{\text{eff}}) + \alpha (\mathbf{m} \times \frac{\partial \mathbf{m}}{\partial t}) - \beta (\mathbf{m} \times (\mathbf{m} \times \mathbf{p}))
\]

Media: \( H_k = 30 \text{ kOe}; \alpha = 0.01 \)
Applied field \( H_a \): 0.2 ns rising time, 2° away vertical direction
AC field \( H_{ac} \): \( H_{ac}/H_k = 0.1 \)
HAMR : Heat Assisted Magnetic Recording

- HAMR is a scalable technology. Opportunity for 1.0 to 4.0 Tbps.
- FePt media allows grain size scaling to support much higher density than PMR
  - Effective field gradient several times higher than PMR → Small grains and high SNR
- Near Field Heating by Laser spot with Write head and making data track < 50nm

\[
\frac{dH_{eff}}{dx} = \frac{dH_k}{dT} \cdot \frac{dT}{dx}
\]
HAMR Media Design

- New magnetic material alloy: FePt.
- High temperature growth needed to form proper crystallographic phase – requires new high-temperature substrate.
- Multiple FePt layers and segregants required for microstructure optimization. Difficult to make as thick as for PMR.
- Minimize the variation of Curie Temperature of each grain.
- Thermal design of heat sink → maximize thermal gradient and minimize power.

\[
\frac{dH_{\text{eff}}}{dx} = \frac{dH_k}{dT} \cdot \frac{dT}{dx}
\]
Comparison: PMR media versus HAMR media

In addition to traditional PMR media parameters, new media parameters become important for HAMR, such as optical and thermal layer design, thermal gradients, Tc, sigma Tc, ...
HAMR media microstructure evolution

- small grains
- tight size distribution
- spherical grains
- low signal
- rough media

- larger grains
- tight size distribution
- more columnar grains
- increased signal
- smoother media

- smaller grains
- tight size distribution
- even more columnar grains
- further increased signal
- smoother media

Newer media
Head-Disk Interface Challenges

Laser Induced Protrusion

- New heat sources (laser diode, scattered light, NFT heating) cause protrusion over various time-scales and length-scales and new challenges for maintaining low head disk spacing and high recording performance.
- High temperatures can cause oxidation (combustion) of thin carbon overcoats on head and disk over the lifetime of a product.
- Intense optical/thermal fields can lead to carbonaceous build up on NFT. Contact can also lead to back heating.

Oxidation of Carbon Overcoats

\[
C(s) + O_2(g) \rightarrow CO_2(g)
\]

Arrhenius Equation

\[ k = A e^{\frac{-E_a}{RT}} \]

Conclusions on HDD

• HDDs will be around for a long time to come
• The modern HDD is packed with high-tech engineering of many disciplines
• Major discoveries at the basic research level enabled the rapid growth of storage capacity
• Energy-assisted recording – MAMR or HAMR – is a promising future technology for recording densities beyond 1Tb/in². Engineering breakthroughs are needed to make it a reality.
Figure 4. (a) Schematic of a spin-transfer-torque magnetoresistive random-access memory bit cell. (b) Cross-sectional transmission electron microscope image of a 20-nm dia. perpendicular magnetic tunnel junction (p-MTJ). Photo courtesy of IBM.
Memory and Storage Hierarchy

- SRAM (Register, Cache)
- DRAM (Main Memory)
- Storage Class Memory
- SSD, Flash Drive (Solid State Memory)
- HDD (Virtual Memory)
HDD vs. Flash SSD $/TB Annual Takedown Trend

MAMR will enable continued $/TB advantage over Flash SSDs

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2D to 3D NAND

Typical 2D NAND FLASH String

Stretch It Out In The Middle

Fold It Over

Stand It Vertically
Flash Technology -- BiCS

BiCS 3D-NAND

BiCS delivers smallest chip area of any published 3D-NAND

- U-shaped NAND string enables maximum array efficiency
- Leverages existing NAND Fab infrastructure. Does not need EUV.
- Scaling achieved by increasing number of layers

Good progress in BiCS development

Challenges for all 3D-NAND manufacturing
- NAND poly TFT devices, a first in volume manufacturing
- High aspect ratio etching of large number of layers and its control
- High volume manufacturing requires new etching equipment and techniques for scaling to high number of layers

Figure: Mass Production Schedules of Major NAND Flash Players

<table>
<thead>
<tr>
<th></th>
<th>2018</th>
<th>2019</th>
<th>2020</th>
</tr>
</thead>
<tbody>
<tr>
<td>SAMSUNG</td>
<td>64L</td>
<td>92L</td>
<td>128L</td>
</tr>
<tr>
<td>SK hynix</td>
<td>72L</td>
<td>96L</td>
<td>128L</td>
</tr>
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<tr>
<td>Intel</td>
<td>64L</td>
<td>96L</td>
<td>128L</td>
</tr>
<tr>
<td>Micron</td>
<td>32L</td>
<td>64L</td>
<td>128L</td>
</tr>
</tbody>
</table>

Notes: From 128L on, Micron will be using Replacement Gate technology different from Intel’s.

Sources: TrendForce, May, 2019

SLC     MLC     TLC     QLC

1       11      111     1111
10      101     1010    10101
01      011     0110    01101
00      001     0010    00101
00      000     0000    00000
Intel Optane
3D Phase Change with Selector

3D XPoint™ Technology: An Innovative, High-Density Design

Cross Point Structure
Perpendicular wires connect microscopic columns. An individual memory cell can be addressed by selecting its top and bottom wire.

Non-Volatile
3D XPoint™ Technology is non-volatile—which means your data won’t go away when your power goes away—making it a great choice for storage.

High Endurance
Unlike other storage memory technologies, 3D XPoint™ Technology is not significantly impacted by the number of write cycles it can endure, making it more durable.

Stackable
These thin layers of memory can be stacked to further boost density.

Selector
Whereas ERAM requires a transistor at each memory cell—making it big and expensive—the amount of voltage sent to each 3D XPoint™ Technology selector enables its memory cell to be written to or read without requiring a transistor.

Memory Cell
Each memory cell can store a single bit of data.
3D Crosspoint

- Access device required for each memory element
  - Eliminate sneak paths
    - Reduce power and unintended selection
    - Apply V/2 on word and bit lines – only V on selected cell
  - Diodes or non-linear I-V devices
  - Unipolar or dipolar depending on memory cell type
STT-MRAM is the only emerging memory technology that combines endurance, speed and energy efficiency of SRAM and DRAM with non-volatility of Flash.

Figure from: A. D. Kent and D. C. Worledge, Nature Nanotech. 10, 187 (2015).

STT-MRAM is the only candidate to replace SRAM in cache memory and DRAM in both embedded and stand alone applications.

STT-MRAM also provides high performance alternative for embedded flash (NOR) in applications where non-volatility is required.

PCM and RRAM are better suited for storage applications where higher density is required and lower endurance and slower speed can be tolerated.
Energy-speed performance of emerging memories

*Based on reported experimental results*

STT-MRAM speed has advantage in terms of speed and energy efficiency over other emerging memory technologies.

MRAM with a magnetic field

More than 20 years ago: Field-MRAM

1st research program: IBM/Motorola (1995)

Issue in scaling – field disturb of half-select bits
No selector!

From S. Parkin and K. Roche IBM
What is a STT-MRAM cell

CMOS transistor + magnetic tunnel junction (MTJ)

Physical sketch:

Symbolic description

Figure from:
D. Apalkov et al.,
Physics of the writing operation

Writing operation of STT-MRAM is based on spin transfer torque switching of the magnetization

Tunneling electrons from one electrode interact with second electrode and are either reflected back or transmitted with new spin orientation. By conservation of angular momentum, the second electrode feels a torque acting upon it. If incoming electric current is high enough, torque can be large enough to switch $\mathbf{m}$.

Landau-Lifshitz-Gilbert-Slonczewski

$$\frac{d\mathbf{m}}{dt} = -\gamma \mu_0 \mathbf{m} \times \mathbf{H} - \alpha \gamma \mu_0 \mathbf{m} \times (\mathbf{m} \times \mathbf{H}) + \gamma \mu_0 \eta \frac{\dot{\mathbf{H}}}{2e M_s t} \mathbf{m} \times (\mathbf{m} \times \mathbf{m}_{RL}) + \gamma \mu_0 \eta' \frac{\dot{\mathbf{m}}}{2e M_s t} \mathbf{m} \times \mathbf{m}_{RL}$$

- $\tau^{\text{STT}}_H$ opposes $\tau_\alpha$ and if large enough it causes switching of the direction of $\mathbf{m}$.
- $\tau^{\text{STT}}_H$ affects precessional frequency, but does not cause switching of $\mathbf{m}$. 
Spin transfer torque switching

Perpendicular vs in-plane magnetic free layer

Perpendicular bits
single uniaxial anisotropy

\[
J_{c0} = \frac{2e\alpha}{\hbar\eta} \mu_0 M_s t H_K
\]

in-plane bits
shape + easy plane anisotropy

\[
J_{c0} = \frac{2e\alpha}{\hbar\eta} \mu_0 M_s t \left( H_K + \frac{H_\perp}{2} \right)
\]

Lower $J_{c0}$ for perpendicular STT-MRAM
=> faster, more power efficient, denser, better endurance than in-plane MRAM

Writing and Reading the magnetization in a MTJ

Write with high current
Read with low current

Write: Spin Transfer Torque
Read: Tunnel Magnetoresistance

Voltage
Resistance

Write [0]
Write [1]
electron flow
electron flow

High R \equiv [1]
Low R \equiv [0]

Courtesy: L. Thomas, MSST 2017
Physics of the non-volatile storage

Non-volatility of STT-MRAM is due to uniaxial magnetic anisotropy of the free (storage) layer $H_k$

For thermally activated magnetization reversal of a single domain particle with uniaxial and easy plane anisotropy only, switching probability $P_{SW}$ over time $t$ is described by the Neel-Brown relaxation time formula with relaxation time $\tau$ and energy barrier $E_b$:

$$P_{SW}(t) = 1 - \exp \left( -\frac{t}{\tau} \right)$$

$$\tau = \tau_0 \exp \left( \frac{E_b}{k_B T} \right)$$

$\tau_0$ - inverse attempt frequency $\sim$ 1 ns

$E_b = \frac{1}{2} \mu_0 M_s H_k V$

$\Delta = \frac{E_b}{k_B T}$ - thermal stability factor

Most applications require $P_{SW} < 10^{-7}$ at elevated temperatures ($> 40 \, ^\circ C$ or more) $\rightarrow \Delta > 60$

Smaller bits need higher magnetic anisotropy in order to maintain the required thermal stability

Impossible to maintain high enough thermal stability with just shape anisotropy below $\sim 60$ nm size

High density applications $\rightarrow$ perpendicular STT-MRAM
Perpendicular STT-MRAM

Due to interfacial perpendicular magnetic anisotropy (iPMA)

Interfacial PMA competes with demagnetization energy
Effective perpendicular magnetic anisotropy is difference between interfacial anisotropy field and demagnetization field
Possible to obtain high enough $H_{K}^{eff}$ to have $\Delta > 70$ for small device size
Materials for Perpendicular STT-MRAM

Yuasa et al, MRS Bulletin May 2018
Recent development of STT-MRAM memories

- Demonstration of stand-alone 4 Gb STT-MRAM main memory (to replace DRAM) by SK Hynix/Toshiba.
  S.-W. Chung et al., IEDM16 - 659 (2016)

- Demonstration of 8Mb 1T-1MTJ STT-MRAM embedded in 28nm CMOS logic (to replace SRAM) by Samsung.
  Y. J. Song et al., IEDM16 - 663 (2016)

Significant development of STT-MRAM for both stand alone and embedded memory platforms.
Embedded MRAM has arrived

June 2017 According to reports, Taiwan Semiconductor Manufacturing Company (TSMC) is aiming to start producing embedded MRAM chips in 2018 using a 22 nm process. This will be initial "risk production" to gauge market reception.

Sept 2017 --- GLOBALFOUNDRIES Announces Availability of Embedded MRAM on Leading 22FDX® FD-SOI Platform

March 2019
SAN FRANCISCO — Samsung announced commercial production of its first embedded MRAM (eMRAM) product based on its 28-nm FD-SOI process.
STT-MRAM challenges

Scaling cell size < 20 nm for high density memories

\[ \Delta = \frac{\mu_0 M_s H_k V}{2k_B T} \]

As volume of the free layer decreases \( H_k \) has to increase in order to maintain the required thermal stability -&gt; increase in iPMA

\[ J_{c0} = \frac{2e\alpha}{\hbar\eta} \mu_0 M_s t H_k \]

Need switching current reduction for lowering power, endurance, higher speed, and shrinking the transistor footprint -&gt; reduced damping \( \alpha \) is crucial and/or Mst

Fabrication of high density memory arrays
-&gt; research into milling and etching methods for MTJs in tight pitch arrays

Maintaining tight distribution of relevant resistances, voltages and \( \Delta s \) at small dimensions
-&gt; materials and process uniformity

Increasing TMR may be required to compensate for wider R distributions

Alternative memory cell designs may be required for sub-10 nm scaling, as well as ultrafast applications that require high endurance and power efficiency, such as cache memories
Distributions

Cell Resistance

Dmytro Apalkov, J. Slaughter
Examples of MRAM Research areas

• Improve STT efficiency
  – Reduce damping and Mst
  – Double MTJ – increase torque
  – Add spin polarization layers

• High Density Patterning
  – Ion beam etching at pitch

• Small devices
  – Shape anisotropy

• Crosspoint MRAM

• SOT and VCMA
Spin orbit torque (SOT)-MRAM

Alternative MRAM cell design for high speed/endurance and power efficiency

<table>
<thead>
<tr>
<th>Storage element</th>
<th>(a) 1T-1R STT-MRAM</th>
<th>(b) 2T-1R SOT-MRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bitcell schematic</td>
<td><img src="image1" alt="Diagram" /></td>
<td><img src="image2" alt="Diagram" /></td>
</tr>
<tr>
<td>Physical Layout Illustration</td>
<td><img src="image3" alt="Diagram" /></td>
<td><img src="image4" alt="Diagram" /></td>
</tr>
</tbody>
</table>

- Basic SOT-MRAM cell:
  - consists of spin-orbit torque layer (typically a heavy metal like Pt, Ta) in contact with MTJ
  - to write current is passed through SOT layer, while to read it is passed through MTJ
  - cell is 3-terminal and requires 2 transistors per cell to controllably write and read

- SOT-MRAM potential advantages:
  - higher endurance (as write voltage is never applied across tunnel barrier)
  - lower write-energy (as write current is applied through low resistance metal instead of high-resistance MTJ)
  - higher writing speed (as higher overdrive current can be applied due to the above)
  - lower write error rate (for the same reason as the above)

Figure from: Y. Kim et al., IEEE Trans. Electron Devices 62, 561 (2015)
Type-x, type-y, type-z SOT devices

<table>
<thead>
<tr>
<th>Type</th>
<th>Type Y</th>
<th>Type X</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMA</td>
<td>In-plane</td>
<td>In-plane</td>
</tr>
<tr>
<td>Highest density</td>
<td>Lower density</td>
<td>Lower density</td>
</tr>
<tr>
<td>fastest</td>
<td>Precessional, slower</td>
<td>fastest</td>
</tr>
<tr>
<td>Highest current</td>
<td>Lowest current</td>
<td>Middle current</td>
</tr>
<tr>
<td>Bias field (x-y)</td>
<td>No field</td>
<td>Bias field (z)</td>
</tr>
</tbody>
</table>

SOT Switching (IMEC)
VCMA (Wang et al, UCLA)

Li et al, MRS Bulletin 2018

VCMA (Wang et al, UCLA)

Requirements

Materials

MgO

Li et al, MRS Bulletin 2018
VoCSM (Toshiba)

$SOT + VCMA$

- The VCMA is used to select the bit to write.
- This can work in a chain; in a cross-point configuration, however, sneak paths would make it impossible to read the bit.
- In theory, this idea gets bit density close to that of a 1T-1R memory, since the large “write” transistor is shared by many bits, and each bit has a small “read” transistor that requires very little current.
- Read can be done in a polarity that helps increase the energy barrier, reducing read disturb.

Fig. 1 A schematic drawing of the VoCSM and the VoCF-writing Scheme
(a) A schematic drawing of one string of the VoCSM
(b) Schematic drawing of the VoCF-writing sequence of (i) and (ii) to write data set of (1,1,0,0,1,0,1,0)
Conclusions on MRAM

- STT-MRAM is the only emerging memory technology that combines endurance, speed and energy efficiency of SRAM and DRAM with non-volatility of Flash
- Working chips have been demonstrated
- Several companies are offering/developing MRAM for embedded and stand alone memory applications
- Further materials, process and device physics developments are needed for pushing the memory cell size below 20 nm, to enable > 10 Gb memory capacities.
- New technology applications are becoming feasible with new physics